SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech I Year II Semester Supplementary Examinations July-2021
DIGITAL LOGIC DESIGN
(Common to CSE & CSIT)

Time: 3 hours

Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1 a Convert the following numbers 3M

    i) $(AB)_{16} = (\quad)_2$

    ii) $(1234)_8 = (\quad)_{16}$

    iii) $(101110.01)_2 = (\quad)_8$

  b Convert the following to binary and then to gray code $(AB33)_{16}$ 4M

  c Perform the following Using BCD arithmetic $(7129)_{10} + (7711)_{10}$ 5M

OR

2 a Simplify the Boolean expressions to minimum number of literals 6M

    (i) $X' + XY + X Z' + XYZ'$

    (ii) $(X+Y) (X+Y')$

  b Express the Boolean function $F = A + B'C$ as a sum of minterms. 6M

UNIT-II

3 a Simplify the Boolean expression using K-map method 6M

    $F(A,B,C,D) = \sum m(1,2,3,8,9,10,11,14) + d(7,15)$

  b Design the circuit by Using NOR gates $F = (X+Y).(X'+Y'+Z')$ 6M

OR

4 a Simplify the following Boolean expression using K-MAP and implement using 7M

    NAND gates. $F(W,X,Y,Z) = XYZ + WXY + WYZ + WXZ$

  b Reduce the expression $F(A,B,C,D) = \pi M(0,2,7,8,9,10,11,15) .d(3,4)$ using K- 5M

    Map.

UNIT-III

5 a Draw and explain the working of a Carry- Look- a-head adder. 6M

  b Implement the following Boolean function using 8:1 multiplexer 6M

    $F(A, B, C, D) = A'BD' + ACD + A'C' D + B'CD$

OR

6   **a** Explain about Decimal Adder.   **7M**

       b Design and draw a full adder circuit.   **5M**

UNIT-IV

7   **a** Draw and explain the operation of D Flip-Flop?   **6M**

       b Explain about Shift Registers?   **6M**

OR

8   **a** What is race-around condition? How does it set eliminate is a Master –slave J-K   **6M**
          flip-flop?

       b Explain the design of a 4 bit binary counter with parallel load in detail.   **6M**

UNIT-V

9   **a** Construct the PROM using the conversion from BCD code to Excess-3 code.   **6M**

       b What is ROM. List the different types of ROMs.   **6M**

OR

10   Design a Combinational circuit using PAL by considering the following Boolean **12M**
        Functions given in sum of minterms:

        $W(A,B,C,D)=\Sigma m\ (2,12,13)$

        $X(A,B,C,D)=\Sigma m\ (7,8,9,10,11,12,13,14,15)$

        $Y(A,B,C,D)=\Sigma m\ (0,2,3,4,5,6,7,8,10,11,15)$

        $Z(A,B,C,D)=\Sigma m\ (1,2,8,12,13)$

*** END ***